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Su et al.

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(54) **DISPLAY AND OPERATING METHOD THEREOF**

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This patent is subject to a terminal disclaimer.

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G09G 3/36 (2006.01)

(52) **U.S. Cl.**
CPC ***G09G 3/3611*** (2013.01); *G09G 2370/08* (2013.01)

(58) **Field of Classification Search**
CPC . H04L 25/0272; H04L 7/0008; H04L 7/033; G09G 3/2096; G09G 5/006; G09G 2330/022; G09G 2370/08; G09G 2370/14; G09G 5/00; G09G 3/36; H03B 1/00
USPC 345/99, 100
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

2004/0117605 A1* 6/2004 Ahmad G06F 11/3648 712/227
2005/0286643 A1* 12/2005 Ozawa H03L 7/087 375/242
2007/0021957 A1* 1/2007 Granger G10L 19/0019 704/200
2010/0148829 A1* 6/2010 Hong G09G 3/3648 327/108
2010/0156885 A1* 6/2010 Cho G09G 3/006 345/214
2013/0050302 A1* 2/2013 Su G09G 3/20 345/691

FOREIGN PATENT DOCUMENTS

TW	525023	3/2003
TW	200632821	9/2006
TW	200632844	9/2006
TW	201117591	5/2011
TW	201312521	3/2013

OTHER PUBLICATIONS

"Office Action of Taiwan Counterpart Application", issued on Dec. 2, 2013, p. 1-p. 19.
"Office Action of Taiwan Counterpart Application", issued on May 26, 2014, p. 1-p. 17.

* cited by examiner

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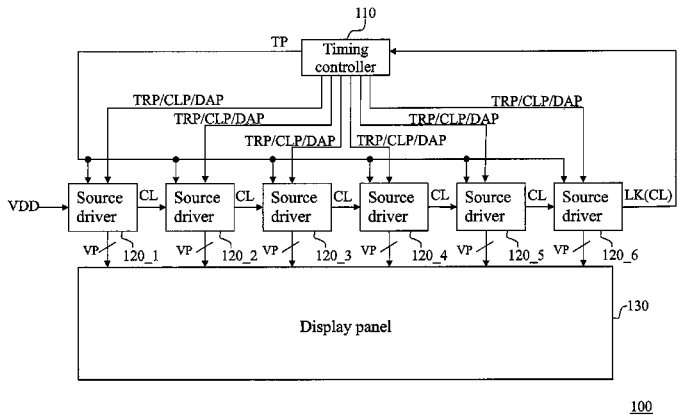
(74) *Attorney, Agent, or Firm* — J.C. Patents

(57) **ABSTRACT**

A display and an operating method thereof are provided. The display includes a display panel, a timing controller, and a plurality of source drivers. The source drivers are coupled to the timing controller and the display panel, and the source drivers are coupled to one another. The timing controller outputs a plurality of training packets to the source drivers. When the source drivers lock a clock of the timing controller according to the training packets, a lock signal is output to the timing controller. The timing controller outputs a plurality of color data packets and at least one latch signal to the source drivers based on the lock signal. The source drivers respectively output a plurality of pixel voltages to the display panel according to the latch signal. The training packets and the color data packets are serially transmitted to the source drivers.

16 Claims, 5 Drawing Sheets



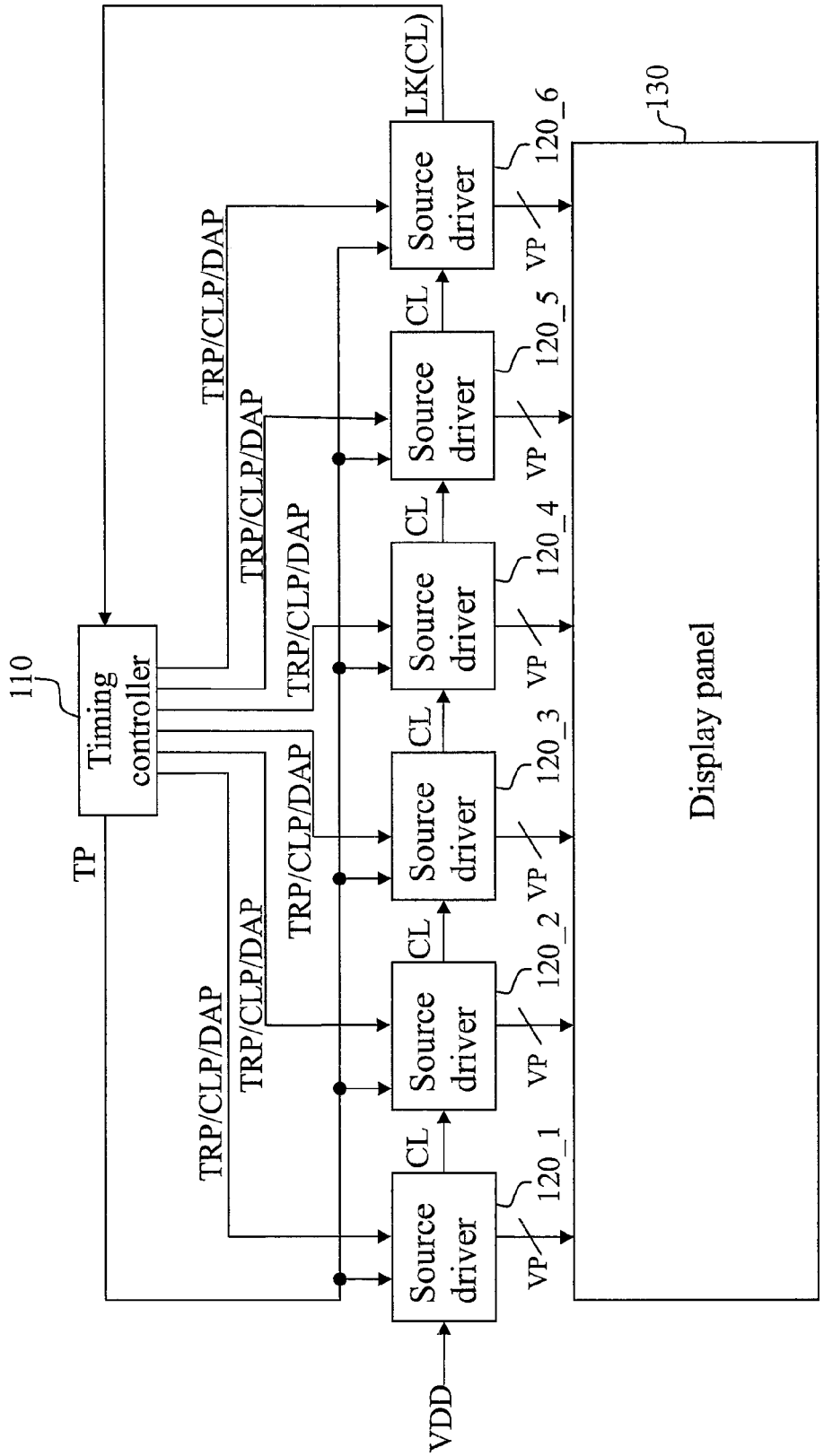

110
Timing controller
TP
VDD
TRP/CLP/DAP
TRP/CLP/DAP
TRP/CLP/DAP
TRP/CLP/DAP
TRP/CLP/DAP
TRP/CLP/DAP
Source driver
CL
VP
120_1
120_2
120_3
120_4
120_5
120_6
LK(CL)
130
Display panel
100

FIG.1

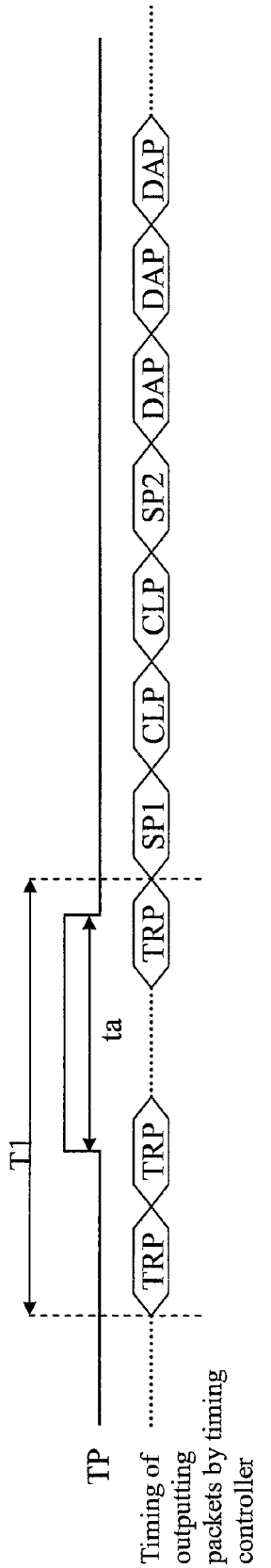


FIG.2

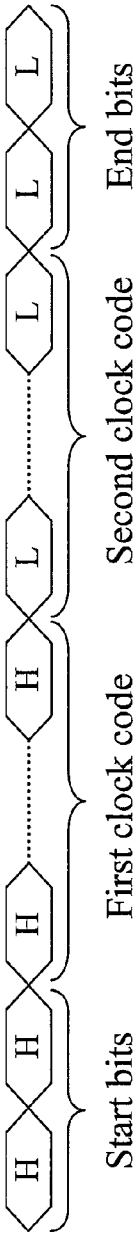


FIG.3

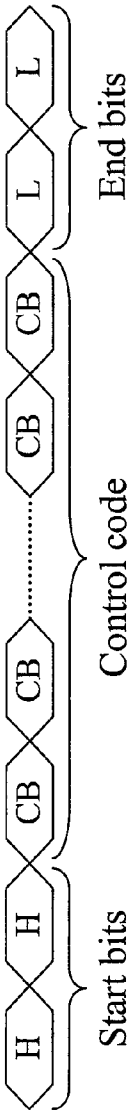


FIG.4

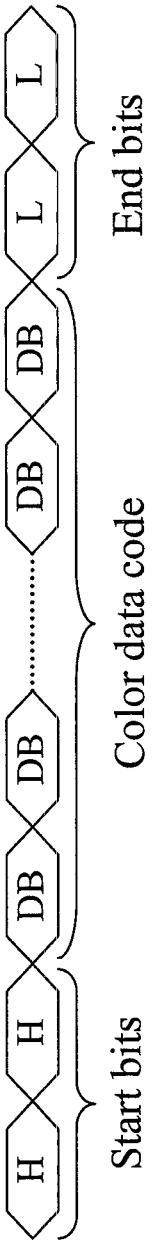


FIG.5

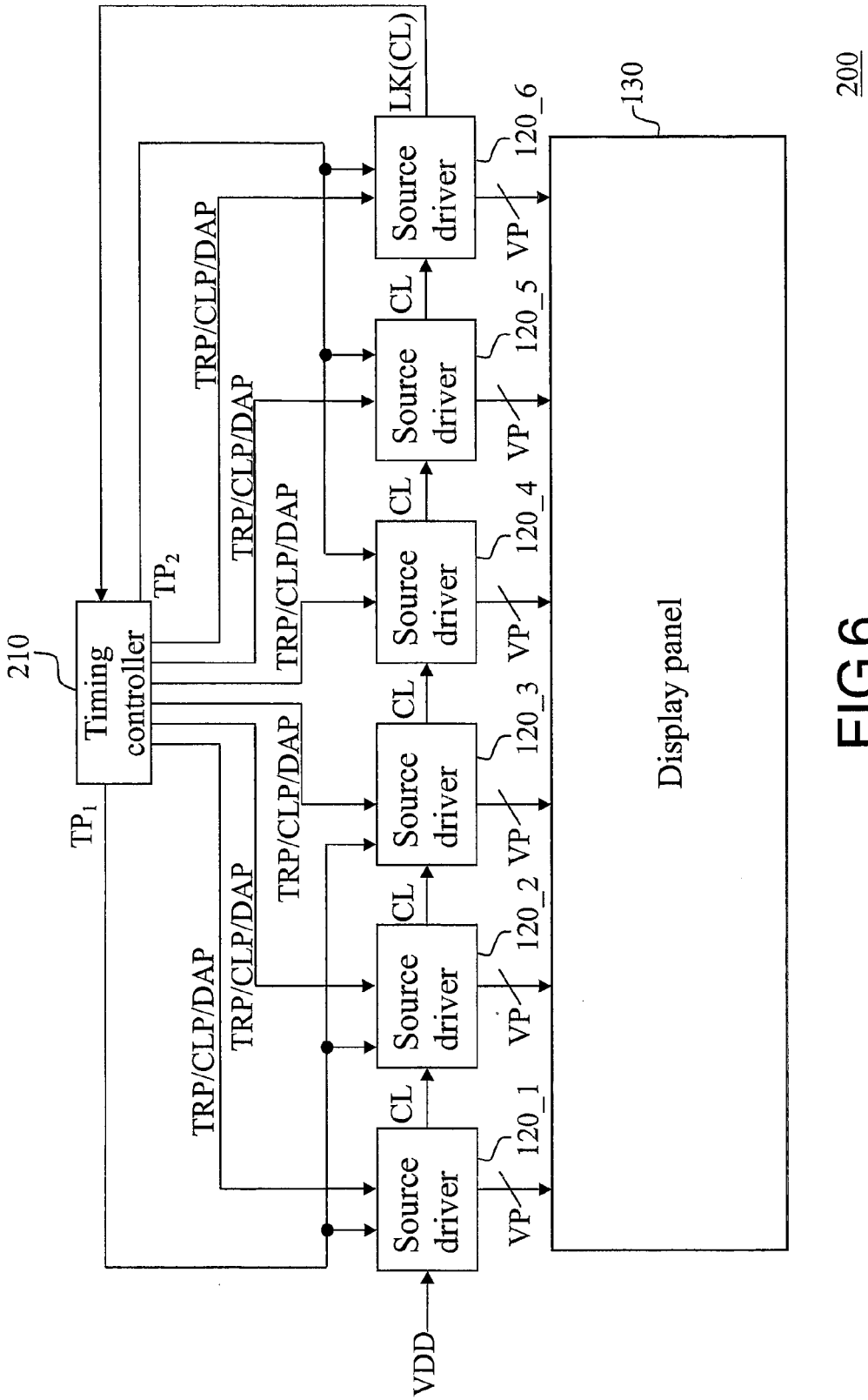

200
210
Timing controller
TP1
TP2
TRP/CLP/DAP
TRP/CLP/DAP
TRP/CLP/DAP
TRP/CLP/DAP
TRP/CLP/DAP
TRP/CLP/DAP
VDD
CL
Source driver
120_1
120_2
120_3
120_4
120_5
120_6
VP
LK(CL)
130
Display panel

FIG.6

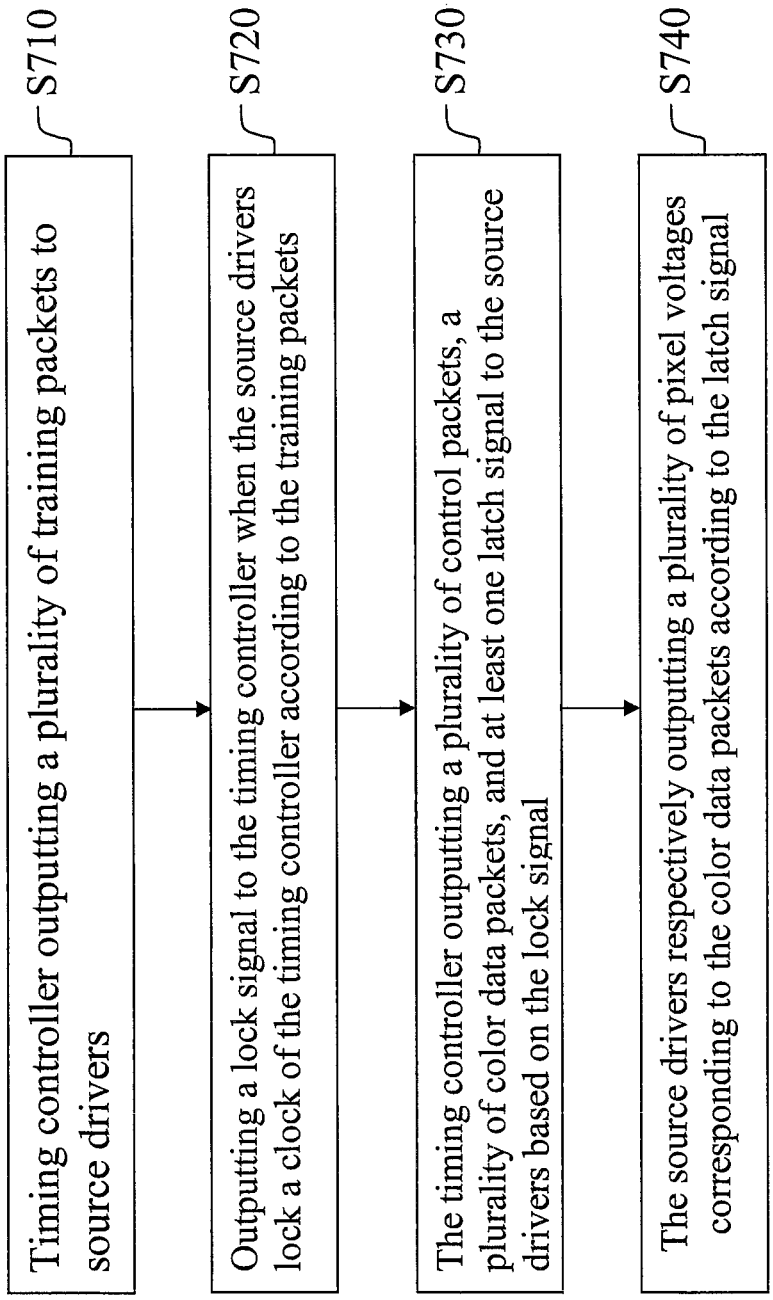

S710
Timing controller outputting a plurality of training packets to source drivers
S720
Outputting a lock signal to the timing controller when the source drivers lock a clock of the timing controller according to the training packets
S730
The timing controller outputting a plurality of control packets, a plurality of color data packets, and at least one latch signal to the source drivers based on the lock signal
S740
The source drivers respectively outputting a plurality of pixel voltages corresponding to the color data packets according to the latch signal

FIG.7

DISPLAY AND OPERATING METHOD THEREOF

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention relates to a display. More particularly, the invention relates to a display in which a timing controller serially transmits data and an operating method of the display.

2. Description of the Related Art

A flat display apparatus, e.g., a thin film transistor liquid crystal display (TFT-LCD), has replaced the conventional cathode ray tube (CRT) display apparatus. Compared to the conventional CRT display, the TFT-LCD display is characterized by various advantages, such as low operating voltage, low power consumption, small volume, small thickness, light weight, etc.

In general, a timing controller and source drivers in a display transmit a control code and color data in parallel. The parallel data transmission contributes to reduction of transmission time, while the number of pins for outputting and receiving signals is increased. Therefore, a printed circuit board (PCB) equipped with both the timing controller and the source drivers has more wires, and the circuit of the PCB is complicated. Since the number of pins cannot be decreased, the chip area cannot be reduced, and thus the hardware costs of the timing controller and the source drivers cannot be lowered down.

SUMMARY OF THE INVENTION

The invention is directed to a display and an operating method thereof. The display has a timing controller and source drivers that are synchronously operated in no need of clock signals. Thereby, the hardware costs of the timing controller and the source drivers can be lowered down.

In an embodiment of the invention, a display that includes a display panel, a timing controller, and a plurality of source drivers is provided. The source drivers are coupled to the timing controller and the display panel, and the source drivers are coupled to one another. The timing controller outputs a plurality of training packets to the source drivers. When the source drivers lock a clock of the timing controller according to the training packets, a lock signal is output to the timing controller. The timing controller outputs a plurality of color data packets and at least one latch signal to the source drivers based on the lock signal. The source drivers respectively output a plurality of pixel voltages corresponding to the color data packets to the display panel according to the latch signals. The training packets and the color data packets are serially transmitted to the source drivers.

According to an embodiment of the invention, the timing controller further outputs a plurality of control packets to the source drivers based on the lock signal.

According to an embodiment of the invention, each of the control packets includes two start bits, two end bits, and a control code that is located between the start bits and the end bits.

According to an embodiment of the invention, the training packets, the color data packets, and the control packets are respectively transmitted by a differential signal.

According to an embodiment of the invention, each of the color data packets includes two start bits, two end bits, and a color data code that is located between the start bits and the end bits.

According to an embodiment of the invention, the color data code corresponds to two of red color data, green color data, and blue color data.

According to an embodiment of the invention, the color data code corresponds to one of red color data, green color data, and blue color data.

According to an embodiment of the invention, the start bits respectively correspond to a logic high level, and the end bits respectively correspond to a logic low level.

According to an embodiment of the invention, each of the training packets includes two start bits, two end bits, a first clock code, and a second clock code. The first clock code is located between the start bits and the second clock code, and the second clock code is located between the first clock code and the end bits.

According to an embodiment of the invention, the start bits and a plurality of bits of the first clock code respectively correspond to a logic high level, and the end bits and a plurality of bits of the second clock code respectively correspond to a logic low level.

According to an embodiment of the invention, when the number of the at least one latch signal is one, the source drivers are controlled by the latch signal and output the pixel voltages.

According to an embodiment of the invention, when the number of the at least one latch signal is two or more, each of the source drivers is respectively controlled by a corresponding one of the latch signals, and the source drivers output the pixel voltages.

In an embodiment of the invention, an operating method of a display is provided. The display includes a display panel, a timing controller, and a plurality of source drivers. The operating method of the display includes following steps. The timing controller outputs a plurality of training packets to the source drivers. When the source drivers lock a clock of the timing controller according to the training packets, a lock signal is output to the timing controller. The timing controller outputs a plurality of color data packets and at least one latch signal to the source drivers based on the lock signal. The source drivers respectively output a plurality of pixel voltages corresponding to the color data packets according to the latch signal. The training packets and the color data packets are serially transmitted to the source drivers.

According to an embodiment of the invention, the source drivers sequentially lock the clock of the timing controller. When the i^{th} source driver locks the clock of the timing controller, the i^{th} source driver outputs a clock lock signal to the source driver, so as to trigger the $(i+1)^{th}$ source driver to lock the clock of the timing controller. When the last source driver of the source drivers locks the clock of the timing controller, the last source driver outputs the lock signal to the timing controller, and the first source driver of the source drivers is triggered by a system voltage to lock the clock of the timing controller. Here, i is greater than or equal to 1 and smaller than the number of the source drivers.

According to an embodiment of the invention, the source drivers lock the clock of the timing controller based on phase comparison.

Based on the above, in the display and the operating method thereof described in the embodiments of the invention, operations of the timing controller and the source drivers can be synchronized due to the training packets. Hence, the timing controller and the source drivers are synchronously operated in no need of the clock signals, and the hardware costs of the timing controller and the source drivers can be lowered down.

Other features and advantages of the invention will be further understood from the further technological features disclosed by the embodiments of the invention wherein there are shown and described embodiments of this invention, simply by way of illustration of modes best suited to carry out the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings are included to provide a further understanding of the disclosure, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the disclosure and, together with the description, serve to explain the principles of the disclosure.

FIG. **1** is a schematic view illustrating a system of a display according to an embodiment of the invention.

FIG. **2** is a schematic timing diagram of a display depicted in FIG. **1** according to an embodiment of the invention.

FIG. **3** is a schematic view illustrating the training packets depicted in FIG. **2** according to an embodiment of the invention.

FIG. **4** is a schematic view illustrating the control packets depicted in FIG. **2** according to an embodiment of the invention.

FIG. **5** is a schematic view illustrating the color data packets depicted in FIG. **2** according to an embodiment of the invention.

FIG. **6** is a schematic view illustrating a system of a display according to another embodiment of the invention.

FIG. **7** is a flowchart illustrating an operating method of a display according to an embodiment of the invention.

DESCRIPTION OF EMBODIMENTS

FIG. **1** is a schematic view illustrating a system of a display according to an embodiment of the invention. With reference to FIG. **1**, in this embodiment, the display **100** includes a timing controller **110**, a plurality of source drivers, and a display panel **130**. In FIG. **1**, six source drivers **120_1~120_6** are exemplarily shown. The timing controller **110** is coupled to the source drivers **120_1~120_6**, so as to output a plurality of training packets TRP, a plurality of control packets CLP, or a plurality of color data packets DAP to the source drivers **120_1~120_6**. The source drivers **120_1~120_6** are coupled to the display panel **130** to respectively output a plurality of pixel voltages VP to the display panel **130**.

In this embodiment, the training packets TRP, the control packets CLP, and the color data packets DAP are serially transmitted by a differential signal. Based on the circuit design of the timing controller **110** and the source drivers **120_1~120_6**, the timing controller **110** can transmit the training packets TRP, the control packets CLP, and the color data packets DAP to the corresponding source drivers (e.g., the source drivers **120_1~120_6**) via one set of differential signal lines or two sets of differential signal lines, which should not be construed as a limitation to the invention.

When the source drivers **120_1~120_6** receive the training packets TRP, the source drivers **120_1~120_6** respectively lock the timing of the training packets TRP to lock a clock of the timing controller **110** based on the training packets TRP received by the source drivers **120_1~120_6**. Here, the source drivers **120_1~120_6** lock the clock of the timing controller **110** based on phase comparison. When each of the source drivers **120_1~120_6** respectively locks the clock of the timing controller **110**, each of the source drivers **120_1~120_6** respectively outputs a clock lock signal CL. When the source drivers **120_1~120_6** all lock the clock of the timing controller **110**, a lock signal LK is output to the timing controller **110**.

In this embodiment, the source drivers **120_1~120_6** sequentially lock the clock of the timing controller **110**. To be more specific, the source driver **120_1** is triggered by a system voltage VDD to lock the clock of the timing controller. When the source driver **120_1** locks the clock of the timing controller **110**, the source driver **120_1** outputs the clock lock signal CL to the source driver **120_2**, so as to trigger the source driver **120_2** to lock the clock of the timing controller **110**. When the source driver **120_2** locks the clock of the timing controller **110**, the source driver **120_2** outputs the clock lock signal CL to the source driver **120_3**, so as to trigger the source driver **120_3** to lock the clock of the timing controller **110**. The rest can be deduced from the above and thus will not be reiterated herein. When the source driver **120_6** locks the clock of the timing controller **110**, the source driver **120_6** outputs the clock lock signal CL (i.e., the lock signal LK) to the timing controller **110**, so as to inform the timing controller **110** of the fact that the source drivers **120_1~120_6** all lock the clock of the timing controller **110**.

When the timing controller **110** receives the lock signal LK, the timing controller **110** outputs the control packets CLP, the color data packets DAP, and a latch signal TP to the source drivers **120_1~120_6** based on the lock signal LK. The source drivers **120_1~120_6** respectively output the pixel voltages VP to the display panel **130** based on the latch signal TP and the color data packets DAP received by the source drivers **120_1~120_6**.

FIG. **2** is a schematic timing diagram of a display depicted in FIG. **1** according to an embodiment of the invention. With reference to FIG. **1** and FIG. **2**, after the source drivers **120_1~120_6** lock the clock of the timing controller **110**, the source drivers **120_1~120_6** can accurately receive the data packets (i.e., the control packets CLP and the color data packets DAP) transmitted by the timing controller **110**. Hence, when the source drivers **120_1~120_6** do not lock the clock of the timing controller **110** (i.e., in the period T**1**), the timing controller **110** transmits the training packets TRP to the source drivers **120_1~120_6**, such that the source drivers **120_1~120_6** can lock the clock of the timing controller **110** based on the training packets TRP.

Besides, the period T**1** is determined based on the time at which the source driver **120_6** outputs the lock signal LK. That is to say, the period T**1** is determined based on the time frame required by all of the source drivers **120_1~120_6** for locking the clock of the timing controller **110**. During the period T**1**, the latch signal TP is enabled, so as to trigger the source drivers **120_1~120_6** to re-position the voltages output by the source drivers **120_1~120_6**. The time to of enabling the latch signal TP is longer than or equal to the time required for transmitting three training packets TRP. Here, the voltages output by the source drivers **120_1~120_6** can be re-positioned by sharing charges, which should however not be construed as a limitation to the invention.

After the source drivers **120_1~120_6** lock the clock of the timing controller **110**, the timing controller **110** transmits a first start packets SP**1** to the source drivers **120_1~120_6**, so as to inform the source drivers **120_1~120_6** of starting transmission of the control packets CLP. After the source drivers **120_1~120_6** received the control packets, the timing controller **110** transmits a second start packets SP**2** to the source drivers **120_1~120_6**, so as to inform the source

drivers **120_1~120_6** of starting transmission of the color data packets DAP. The timing controller **110** then outputs the control packets CLP to the source drivers **120_1~120_6**, so as to determine the operational mode or the parameters of the source drivers **120_1~120_6**. Alternatively, the source drivers **120_1~120_6** output the color data packets DAP to the source drivers **120_1~120_6**, and the source drivers **120_1~120_6** output the pixel voltages VP based on the color data packets DAP received by the source drivers **120_1~120_6**.

After the source drivers **120_1~120_6** receive sufficient color data packets DAP, the timing controller **110** enables the latch signal TP, such that the timing controller **110** can determine the timing at which the source drivers **120_1~120_6** output the pixel voltages VP. Thereby, the source drivers **120_1~120_6** and the timing controller **110** can be synchronously operated in no need of clock signals, and the number of the pins of the source drivers **120_1~120_6** and the timing controller **110** can be reduced. As such, the hardware costs of the source drivers **120_1~120_6** and the timing controller **110** can be lowered down.

FIG. **3** is a schematic view illustrating the training packets depicted in FIG. **2** according to an embodiment of the invention. With reference to FIG. **3**, in this embodiment, each of the training packets TRP includes two start bits, two end bits, a first clock code, and a second clock code. The bit number of the first clock code is equal to the bit number of the first clock code. The first clock code is located between the start bits and the second clock code, and the second clock code is located between the first clock code and the end bits. Here, the start bits and the bits of the first clock code respectively correspond to a logic high level H, and the end bits and the bits of the second clock code respectively correspond to a logic low level L, such that the training packets TRP are logically equal to a pulse of the clock signal.

FIG. **4** is a schematic view illustrating the control packets depicted in FIG. **2** according to an embodiment of the invention. With reference to FIG. **4**, in this embodiment, each of the control packets CLP includes two start bits, two end bits, and a control code located between the start bits and the end bits. The control code is constituted by a plurality of control data bits CB. Besides, the start bits respectively correspond to a logic high level H, and the end bits respectively correspond to a logic low level L.

FIG. **5** is a schematic view illustrating the color data packets depicted in FIG. **2** according to an embodiment of the invention. With reference to FIG. **5**, in the embodiment of the invention, each of the color data packets DAP includes two start bits, two end bits, and a color data code located between the start bits and the end bits. The color data code is constituted by a plurality of color data bits DB. The start bits respectively correspond to the logic high level H, and the end bits respectively correspond to the logic low level L.

In this embodiment, the color data code corresponds to two of red color data, green color data, and blue color data, or the color data code corresponds to one of red color data, green color data, and blue color data. People having ordinary skill in the art may make modifications accordingly.

Besides, in this embodiment, the packet size of the training packets TRP, the control packets CLP, and the color data packets DAP is the same (i.e., the bit number of these packets is the same). If each of the color data is assumed to be 10 bits, and the color data code corresponds to two of the red color data, the green color data, and the blue color data, the training packets TRP, the control packets CLP, and the color data packets DAP are 24 bits (i.e., 2+10+10+2). If each of the color data is assumed to be 10 bits, and the color data code corresponds to one of the red color data, the green color data, and the blue color data, the training packets TRP, the control packets CLP, and the color data packets DAP are 14 bits (i.e., 2+10+2).

If each of the color data is assumed to be 8 bits, and the color data code corresponds to two of the red color data, the green color data, and the blue color data, the training packets TRP, the control packets CLP, and the color data packets DAP are 20 bits (i.e., 2+8+8+2). If each of the color data is assumed to be 8 bits, and the color data code corresponds to one of the red color data, the green color data, and the blue color data, the training packets TRP, the control packets CLP, and the color data packets DAP are 12 bits (i.e., 2+8+2).

If each of the color data is assumed to be 6 bits, and the color data code corresponds to two of the red color data, the green color data, and the blue color data, the training packets TRP, the control packets CLP, and the color data packets DAP are 16 bits (i.e. 2+6+6+2). If each of the color data is assumed to be 6 bits, and the color data code corresponds to one of the red color data, the green color data, and the blue color data, the training packets TRP, the control packets CLP, and the color data packets DAP are 10 bits (i.e. 2+6+2).

FIG. **6** is a schematic view illustrating a system of a display according to another embodiment of the invention. With reference to FIG. **1** and FIG. **6**, the display **200** of this embodiment is similar to the display **100** depicted in FIG. **1**, while the difference therebetween lies in that the timing controller **210** outputs two latch signals TP_1 and TP_2. The source drivers **120_1~120_3** are controlled by the latch signal TP_1 and output the pixel voltages VP, and the source drivers **120_4~120_6** are controlled by the latch signal TP_2 and output the pixel voltages VP. In other words, the source drivers **120_1~120_6** are respectively controlled by the latch signals TP_1 and TP_2 and output the pixel voltages VP. Similarly, when the timing controller **210** outputs a plurality of latch signals, the source drivers (e.g., the source drivers **120_1~120_6**) are respectively controlled by the corresponding latch signals and output the pixel voltages.

FIG. **7** is a flowchart illustrating an operating method of a display according to an embodiment of the invention. With reference to FIG. **7**, the display of this embodiment includes a timing controller and a plurality of source drivers. The timing controller outputs a plurality of training packets to the source drivers (step **S710**). When the source drivers lock a clock of the timing controller according to the training packets, a lock signal is output to the timing controller (step **S720**). The timing controller outputs a plurality of control packets, a plurality of color data packets, and at least one latch signal to the source drivers based on the lock signal (step **S730**). Here, the training packets and the color data packets are serially transmitted to the source drivers. The source drivers respectively output a plurality of pixel voltages corresponding to the color data packets according to the latch signals (step **S740**). The above-mentioned order of performing said steps is exemplary and should not be construed as a limitation to the invention. The detailed steps can be referred to as those described above with respect to the displays **100** and **200** and thus are not reiterated herein.

To sum up, in the display and the operating method thereof described in the embodiments of the invention, the timing controller and the source drivers are synchronously operated due to the training packets. Hence, the timing controller and the source drivers are synchronously operated

in no need of the clock signals, and the hardware costs of the timing controller and the source drivers can be lowered down.

It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the disclosed embodiments without departing from the scope or spirit of the disclosure. In view of the foregoing, it is intended that the disclosure covers modifications and variations of this disclosure provided they fall within the scope of the following claims and their equivalents.

What is claimed is:

1. A display comprising:

a display panel;

a timing controller; and

a plurality of source drivers coupled to the timing controller and the display panel, the source drivers being coupled to one another,

wherein the timing controller outputs a plurality of training packets to the source drivers for locking a clock of the timing controller, and latch signal is enabled during locking the clock of the timing controller, so as to trigger the source drivers to re-position voltages output by the source drivers, when the source drivers lock the clock of the timing controller based on the training packets, a lock signal is output to the timing controller, the timing controller outputs a plurality of color data packets and the latch signal to the source drivers based on the lock signal when the timing controller receives the lock signal, the source drivers respectively output a plurality of pixel voltages corresponding to the color data packets to the display panel based on the latch signal, and the training packets and the color data packets are serially transmitted to the source drivers,

wherein the timing controller transmits a first start packet to the source drivers after the source drivers lock the clock of the timing controller to signal the transmission of control packets, the timing controller transmits a second start packet to the source drivers after the source drivers receive the control packets to signal the transmission of the color data packets, and the timing controller enables the latch signal after the color data packets are received by the source drivers, so as to determine a timing at which the source drivers output the pixel voltages,

wherein the timing controller outputs the plurality of control packets to the source drivers based on the lock signal, and each of the control packets comprises two start bits, two end bits, and a control code located between the start bits and the end bits.

2. The display as recited in claim **1**, the source drivers sequentially locking the clock of the timing controller, wherein when an ith source driver of the source drivers locks the clock of the timing controller, the ith source driver outputs a clock lock signal to an (i+1)th source driver of the source drivers, so as to trigger the (i+1)th source driver to lock the clock of the timing controller, and when a last source driver of the source drivers locks the clock of the timing controller, the last source driver outputs the lock signal to the timing controller, and a first source driver of the source drivers is triggered by a system voltage to lock the clock of the timing controller, i being greater than or equal to 1 and smaller than the number of the source drivers.

3. The display as recited in claim **1**, wherein the start bits respectively correspond to a logic high level, and the end bits respectively corresponding to a logic low level.

4. The display as recited in claim **1**, wherein the training packets, the color data packets, and the control packets are respectively transmitted by a differential signal.

5. The display as recited in claim **1**, wherein each of the color data packets comprises two start bits, two end bits, and a color data code located between the start bits and the end bits.

6. The display as recited in claim **5**, wherein the color data code corresponds to two of red color data, green color data, and blue color data.

7. The display as recited in claim **5**, wherein the color data code corresponds to one of red color data, green color data, and blue color data.

8. The display as recited in claim **5**, wherein the start bits respectively correspond to a logic high level, and the end bits respectively corresponding to a logic low level.

9. The display as recited in claim **1**, wherein each of the training packets comprises two start bits, two end bits, a first clock code, and a second clock code, the first clock code is located between the start bits and the second clock code, and the second clock code is located between the first clock code and the end bits.

10. The display as recited in claim **9**, wherein the start bits and a plurality of bits of the first clock code respectively correspond to a logic high level, and the end bits and a plurality of bits of the second clock code respectively correspond to a logic low level.

11. The display as recited in claim **1**, wherein the source drivers lock the clock of the timing controller based on phase comparison.

12. The display as recited in claim **1**, wherein when the number of the latch signal is one, the source drivers are controlled by the latch signal and output the pixel voltages.

13. The display as recited in claim **1**, wherein when the number of the latch signals is two or more, each of the source drivers is respectively controlled by a corresponding one of the latch signals, and the source drivers output the pixel voltages.

14. An operating method of a display, the display comprising a timing controller and a plurality of source drivers, the operating method comprising:

outputting a plurality of training packets to the source drivers for locking a clock of the timing controller, and latch signal is enabled during locking the clock of the timing controller, so as to trigger the source drivers to re-position voltages output by the source drivers by using the timing controller;

outputting a lock signal to the timing controller when the source drivers lock the clock of the timing controller according to the training packets;

when the timing controller receives the lock signal, outputting a plurality of color data packets and the latch signal to the source drivers based on the lock signal by using the timing controller;

respectively outputting a plurality of pixel voltages corresponding to the color data packets according to the latch signal by using the source drivers; and

outputting a plurality of control packets to the source drivers based on the lock signal by using the timing controller,

wherein the training packets and the color data packets are serially transmitted to the source drivers,

wherein a first start packet is transmitted to the source drivers after the source drivers lock the clock of the timing controller to signal the transmission of the control packets, a second start packet is transmitted to the source drivers after the source drivers receive the

control packets to signal the transmission of the color data packets, and the timing controller.

15. The operating method of the display as recited in claim **14**, the source drivers sequentially locking the clock of the timing controller, wherein when an ith source driver of the source drivers locks the clock of the timing controller, the ith source driver outputs a clock lock signal to an (i+1)th source driver of the source drivers, so as to trigger the (i+1)th source driver to lock the clock of the timing controller, and when a last source driver of the source drivers locks the clock of the timing controller, the last source driver outputs the lock signal to the timing controller, and a first source driver of the source drivers is triggered by a system voltage to lock the clock of the timing controller, i being greater than or equal to 1 and smaller than the number of the source drivers.

16. The operating method of the display as recited in claim **14**, wherein the source drivers lock the clock of the timing controller based on phase comparison.

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